ACCUMULATOR SHADOW REGISTER SYSTEMS AND METHODS

ABSTRACT OF THE DISCLOSURE

Systems and methods are disclosed for facilitating communication between execution units in a processor. In one embodiment, an integer unit is provided with a set of shadow registers corresponding to each of a plurality of datapath units. Each shadow register is communicatively coupled to a datapath unit, and contains a copy of the contents of the datapath unit's accumulator register. When data is written to a datapath unit's accumulator register, it is also written to a shadow register in the integer unit, where it can be used by the integer unit in further computations.